In the specification:

Please replace the original paragraphs with following paragraphs:

[0018] Above the gates, cobalt silicide formations [127] 126 are grown around the top of the control gate and an etch stop silicon nitride (Si_3N_4) layer 129 is formed to cover the entire transistor structure. The silicon nitride layer covers the cobalt silicide formations, the control and floating gates, the liner oxide, and the nitride spacers. After the transistor structure has been etched and cleaned, an inter-layer dielectric layer 131 covers the entire structure.

[0028] After the second portion is formed, the silane flow is diverted from the chamber ~~at block 328~~, and, after 0.5 seconds or longer, the plasma is turned off at block 329. At block 331, residue gases in the chamber are purged out to the pump again. The wafer may then be moved again and the sequence may be continued at block 333 until the complete layer is formed.

[0036] The MCH chip 963 is also coupled to an ICH (Input/Output controller hub) chip 965. The ICH chip offers connectivity to a wide range of different devices. Well-established conventions and protocols may be used for these connections. The connections may include a LAN (Local Area Network) port [69] 969, a USB hub 971, and the local BIOS (Basic Input/Output System) flash memory 973. A SIO (Super Input/Output) port 975 may provide connectivity for a keyboard or other input devices.